

PROFESSIONAL SUMMARY

- An enthusiastic Electrical Engineer, deeply passionate about **Analog IC design**, with a background in the **SerDes** industry and **ADC** design
- Designed and **taped-out** analog blocks of a Low-Area Low-Power CT Δ - Σ ADC for CMOS image sensors
- Gained valuable leadership skills by **leading an IC design capstone team**, collaborating with **multiple Analog + Digital designers** and proactively engaging with project sponsor on system integration, design schedule/targets etc. from concept to tape-out
- Thorough academic learning of device fundamentals, modelling, and non-idealities. Took **graduate-level Analog IC and RFIC Design** course (Projects: Gm-C integrator, 10GHz LC-VCO)
- Proficient in **Cadence Virtuoso** through graduate-level semester projects and previous work experience. Well-versed in **MATLAB** modelling, **Python** and **Ocean** scripting
- Well-versed in **lab measurements** using VNAs, BERT, spectrum analyzers, high-BW scopes, function generators and DAQs
- Open to relocation within North America

TECHNICAL PROFICIENCIES

Design & Simulation Tools

- Virtuoso, ADEXL, Maestro
- Mentor Calibre
- MATLAB / Simulink
- LTspice
- Xcellium, VCS, ModelSim

Languages

- Python
- VHDL, Verilog-A
- C / C++
- Ocean, TCL

PCB Design Tools

- Altium
- Zuken Cadstar

EDUCATION

BSc. Electrical Engineering

2017 – 2022

University of Calgary | GPA: 3.86 / 4.00 | Minor: Computer Engineering

- Relevant courses: Analog IC Design, RFIC Design, CMOS Image Sensors, Computer Architecture
- 3x Dean's List Honouree. Graduated with Distinction and 16-month internship

Scholarships

2020 International Undergraduate Award → 20 awards annually among a cohort of 800 Engineering students

2019 Nic Topps Memorial Scholarship → Only 1 award annually among a cohort of 150 Electrical Engineering students

2018 Dr. Gregory Shaw Scholarship → Only 3 awards annually among a cohort of 150 Electrical Engineering students

2018 PURE Undergraduate Research Award

PROJECTS

A 1MSPS 8.33-bit ENOB Low-Area CT Δ - Σ ADC for CMOS Imagers in TSMC 130nm (Capstone project)

- Objective: To design a 1.2V low-area low-power ADC for novel wide-DR CMOS image sensor in TSMC 130nm.
- Completed literature review and modelled 1st order Δ - Σ architecture in MATLAB Simulink to analyze analog modulator and digital filter trade-offs and sub-block specs
- Designed all analog ADC sub-blocks in Virtuoso such as Gm-C transconductor, high-speed comparator, current-steering DAC, and a voltage reference
- Converted single-ended voltage summation Δ - Σ architecture (first design iteration) to differential current summation architecture (final design iteration)
- Optimized modulator sampling rate and power consumption, analog layout area and modulator SNDR

- Led the analog design team consisting of two layout team members and coordinated analog-digital integration efforts with three other digital design team members. Also worked with a graduate student (Devin Atkin) for integration of novel image sensor, chip floorplan and tape-out.
- For project target and achieved specifications, please view [project details](#)

A Low-Power 10GHz LC VCO With Digital Tuning for High-Speed Wireline Transceivers in TSMC 130nm

- Objective: To design a low-phase noise and wide tuning-range VCO for 10-25Gbps Serdes links in TSMC 130nm.
- Analyzed and optimized a variety of design aspects of LC-VCO such as cyclo-stationary and tail PN, output voltage swing, gain, tuning range, power consumption, parasitics, effects of lossy varactors and inductor Q
- Added distributed switched capacitors to VCO architecture for wider tuning range and studied impacts of additional device parasitics.
- Prepared performance comparison with other published works and presented the design to course instructor, Dr. Leonid Belostotski ([View project details](#))

Specification	This project **	Units
Center Frequency	10	GHz
Topology	LC Cross-Coupled NMOS	-
Tuning Range	10.8	%
Power Consumption (VCO core)	1.872	mW
Phase Noise @ 1MHz offset	-103.7	dBc/Hz
Phase Noise @ 10MHz offset	-123.9	dBc/Hz
Output Voltage Pk-Pk	0.429	V
Start-up time	2.34	ns

WORK EXPERIENCE

High-Speed Serdes Applications Engineer

2022(May) – current

Rambus (now Cadence), Toronto

- Worked with analog designers on TX/RX design verification for 22nm multi-protocol SerDes IP
- Gained familiarity with the functionality of various SerDes sub-blocks such as LC and RPLLs, CDR, CTLE, CMU, Lane TX/RX architecture etc.
- Streamlined SerDes IBIS-AMI simulations, DPI+CPU simulations, and PI simulations for various PCIe PHY IPs
- Proactively managed client relations and served a diverse clientele across 3 continents spanning from start-ups to Fortune 500 companies, with a focus on multiple sectors including Military, Space and Data Centers
- Demonstrated a consistent track record of debugging complex SerDes customer issues in a constrained timeframe and with limited information. Accumulated 1900+ hours of SerDes client interaction

Hardware Design Engineer (16-Month Internship)

2020(May) – 2021(Aug)

Garmin Inc., Calgary

- Designed cutting-edge fitness products with 2.4GHz connectivity such as pro-athletic cycling/swimming electronics
- Led simulation, schematic, layout, and manufacturing team reviews for upcoming products
- Effectively communicated design constraints (part cost, component placement, design time, materials, and manufacturing etc.) to other engineering teams, managers, silicon vendors and manufacturing facilities
- Successfully developed product concept, margin analysis and overall project schedules with senior management
- Link to a released Garmin product that I designed: [Garmin Powered Mount](#)

Lifecycle Engineer (4-Month Internship)

2019(May) – 2019(Aug)

AltaLink, Calgary

- Developed optimized Python scripts for Alberta's electrical grid maintenance, significantly reducing 4.1 months of manual work to 2 hours

* Post-layout simulation results

** Pre-layout simulation results